



## Device Overview

The 89HPES12NT3 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES12NT3 is a 12-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCIe® upstream port, a transparent downstream port, and a non-transparent downstream port.

With non-transparent bridging (NTB) functionality, the PES12NT3 can be used standalone or as a chipset with IDT PCIe System Interconnect Switches in multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

## Features

- ◆ **High Performance PCI Express Switch**
  - Twelve PCI Express lanes (2.5Gbps), three switch ports
  - Delivers 48 Gbps (6 GBps) of aggregate switching capacity
  - Low latency cut-through switch architecture
  - Support for Max Payload size up to 2048 bytes
  - Supports one virtual channel and eight traffic classes
  - PCI Express Base specification Revision 1.0a compliant

- ◆ **Flexible Architecture with Numerous Configuration Options**
  - Port arbitration schemes utilizing round robin
  - Supports automatic per port link width negotiation (x4, x2, or x1)
  - Static lane reversal on all ports
  - Automatic polarity inversion on all lanes
  - Supports locked transactions, allowing use with legacy software
  - Ability to load device configuration from serial EEPROM
  - Ability to control device via SMBus
- ◆ **Non-Transparent Port**
  - Crosslink support on NTB port
  - Four mapping windows supported
    - Each may be configured as a 32-bit memory or I/O window
    - May be paired to form a 64-bit memory window
  - Interprocessor communication
    - Thirty-two inbound and outbound doorbells
    - Four inbound and outbound message registers
    - Two shared scratchpad registers
  - Allows up to sixteen masters to communicate through the non-transparent port
  - No limit on the number of supported outstanding transactions through the non-transparent bridge
  - Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
  - Supports direct connection to a transparent or non-transparent port of another switch

## Block Diagram

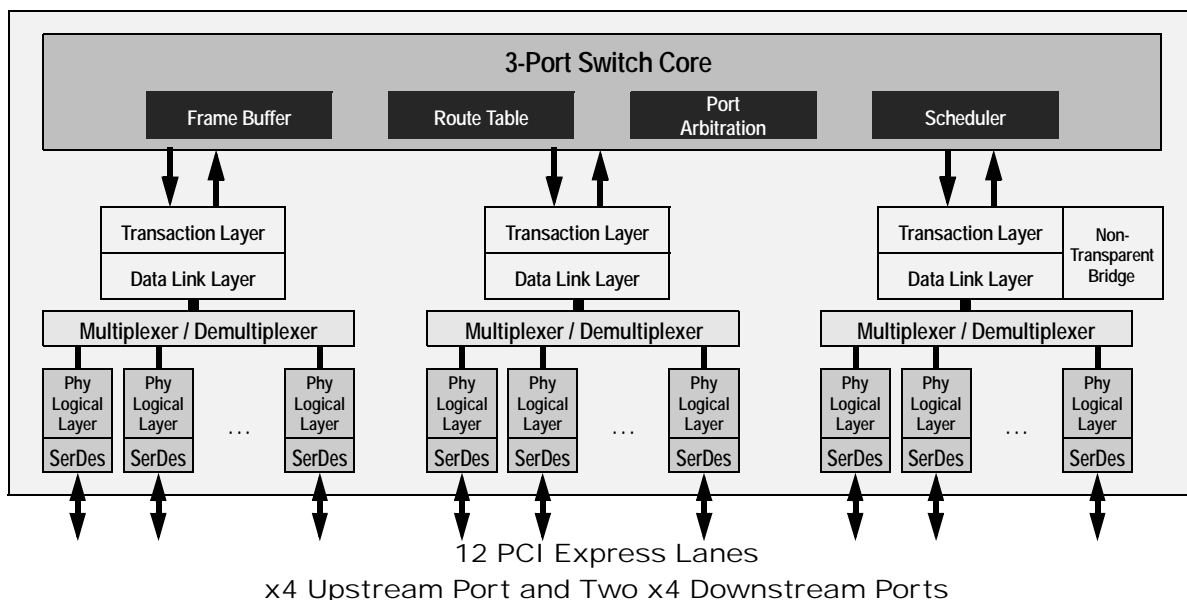


Figure 1 Internal Block Diagram

IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc.

- ◆ **Highly Integrated Solution**
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates twelve 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)
- ◆ **Reliability, Availability, and Serviceability (RAS) Features**
  - Upstream port can be dynamically swapped with non-transparent downstream port to support failover applications
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports ECRC pass-through in transparent and non-transparent ports
  - Supports Hot-Swap
- ◆ **Power Management**
  - Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
  - Unused SerDes are disabled
- ◆ **Testability and Debug Features**
  - Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
  - Ability to read and write any internal register via the SMBus
  - Ability to bypass link training and force any link into any mode
  - Provides statistics and performance counters
- ◆ **Two SMBus Interfaces**
  - Slave interface provides full access to all software-visible registers by an external SMBus master
  - Master interface provides connection for an optional serial EEPROM used for initialization
  - Master interface is also used by an external Hot-Plug I/O expander
  - Master and slave interfaces may be tied together so the switch can act as both master and slave
- ◆ **Eight General Purpose Input/Output pins**
- ◆ **Packaged in 19x19mm 324-ball BGA with 1mm ball spacing**

## Product Description

Utilizing standard PCI Express interconnect, the PES12NT3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES12NT3, as a standalone switch or as a chipset with IDT PCIe System Interconnect Switches, enables multi-host and intelligent I/O applications requiring inter-domain communication. The PES12NT3 provides 48 Gbps (6 GBps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12NT3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12NT3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource

management. This includes round robin port arbitration, guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 GbE I/Os, SATA controllers, and Fibre Channel HBAs.

## Switch Configuration

The PES12NT3 is a three port switch that contains 12 PCI Express lanes. Each of the three ports is statically allocated 4 lanes with ports labeled as A, B and C. Port A is the upstream port, port B is the transparent downstream port, and port C is the non-transparent downstream port.

During link training, link width is automatically negotiated. Each PES12NT3 port is capable of independently negotiating to a x4, x2 or x1 width. Thus, the PES12NT3 may be used in virtually any three port switch configuration (e.g., {x4, x4, x4}, {x4, x2, x2}, {x4, x2, x1}, etc.). The PES12NT3 supports static lane reversal. For example, lane reversal for upstream port A may be configured by asserting the PCI Express Port A Lane Reverse (PEALREV) input signal or through serial EEPROM or SMBus initialization. Lane reversal for ports B and C may be enabled via a configuration space register, serial EEPROM, or the SMBus.

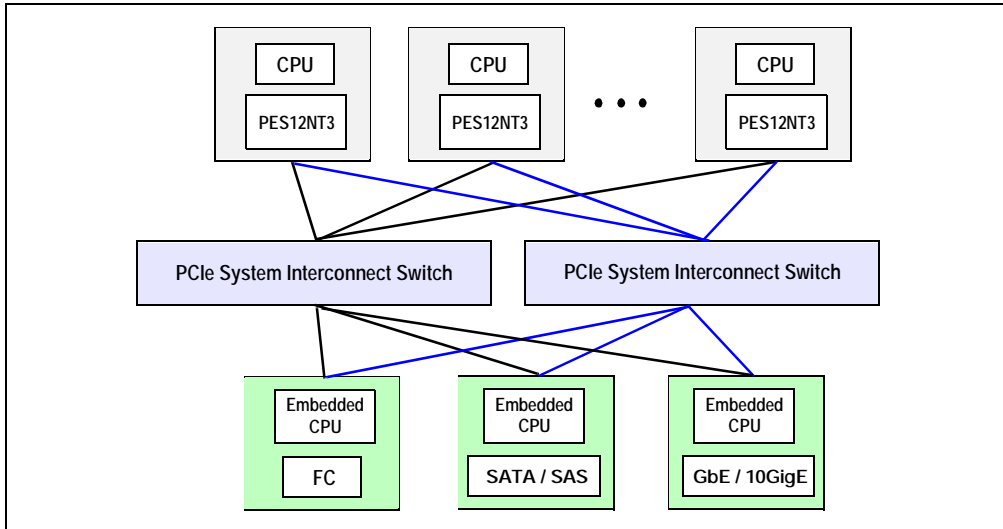


Figure 2 PCIe System Interconnect Architecture Block Diagram

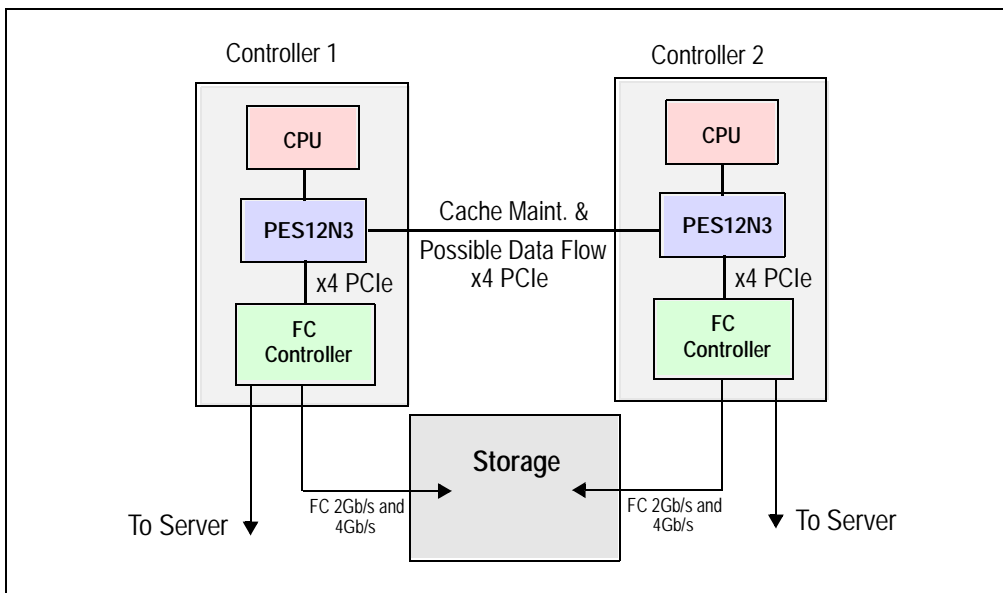


Figure 3 Dual Host Storage System

## Pin Description

The following tables list the functions of the pins provided on the PES12NT3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

| Signal                           | Type | Name/Description   |
|----------------------------------|------|--|
| PEALREV                          | I    | <b>PCI Express Port A Lane Reverse.</b> When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.   |
| PEARP[3:0]<br>PEARN[3:0]         | I    | <b>PCI Express Port A Serial Data Receive.</b> Differential PCI Express receive pairs for port A.  |
| PEATP[3:0]<br>PEATN[3:0]         | O    | <b>PCI Express Port A Serial Data Transmit.</b> Differential PCI Express transmit pairs for port A   |
| PEBLREV                          | I    | <b>PCI Express Port B Lane Reverse.</b> When this bit is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register.   |
| PEBRP[3:0]<br>PEBRN[3:0]         | I    | <b>PCI Express Port B Serial Data Receive.</b> Differential PCI Express receive pairs for port B.  |
| PEBTP[3:0]<br>PEBTN[3:0]         | O    | <b>PCI Express Port B Serial Data Transmit.</b> Differential PCI Express transmit pairs for port B   |
| PECLREV                          | I    | <b>PCI Express Port C Lane Reverse.</b> When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.   |
| PECRP[3:0]<br>PECRN[3:0]         | I    | <b>PCI Express Port C Serial Data Receive.</b> Differential PCI Express receive pairs for port C.  |
| PECTP[3:0]<br>PECTN[3:0]         | O    | <b>PCI Express Port C Serial Data Transmit.</b> Differential PCI Express transmit pairs for port C   |
| PEREFCLKP[1:0]<br>PEREFCLKN[1:0] | I    | <b>PCI Express Reference Clock.</b> Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal. |
| REFCLKM                          | I    | <b>PCI Express Reference Clock Mode Select.</b> These signals select the frequency of the reference clock input.<br>0x0 - 100 MHz<br>0x1 - 125 MHz   |

Table 1 PCI Express Interface Pins

| Signal        | Type | Name/Description   |
|---------------|------|--|
| MSMBADDR[4:1] | I    | <b>Master SMBus Address.</b> These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.   |
| MSMBCLK       | I/O  | <b>Master SMBus Clock.</b> This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed. |
| MSMBDAT       | I/O  | <b>Master SMBus Data.</b> This bidirectional signal is used for data on the master SMBus.  |

Table 2 SMBus Interface Pins (Part 1 of 2)

| Signal          | Type | Name/Description  |
|-----------------|------|---|
| SSMBADDR[5,3:1] | I    | <b>Slave SMBus Address.</b> These pins determine the SMBus address to which the slave SMBus interface responds. |
| SSMBCLK         | I/O  | <b>Slave SMBus Clock.</b> This bidirectional signal is used to synchronize transfers on the slave SMBus.        |
| SSMBDAT         | I/O  | <b>Slave SMBus Data.</b> This bidirectional signal is used for data on the slave SMBus.                         |

Table 2 SMBus Interface Pins (Part 2 of 2)

| Signal  | Type | Name/Description   |
|---------|------|--|
| GPIO[0] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PEBRSTN<br>Alternate function pin type: Output<br>Alternate function: Reset output for downstream port B |
| GPIO[1] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PECRSTN<br>Alternate function pin type: Output<br>Alternate function: Reset output for downstream port C |
| GPIO[2] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PALINKUPN<br>Alternate function pin type: Output<br>Alternate function: Port A link up status output     |
| GPIO[3] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PBLINKUPN<br>Alternate function pin type: Output<br>Alternate function: Port B link up status output     |
| GPIO[4] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PCLINKUPN<br>Alternate function pin type: Output<br>Alternate function: Port C link up status output     |
| GPIO[5] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: FAILOVERP<br>Alternate function pin type: Input<br>Alternate function: NTB upstream port failover        |
| GPIO[6] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.  |
| GPIO[7] | I/O  | <b>General Purpose I/O.</b><br>This pin can be configured as a general purpose I/O pin.  |

Table 3 General Purpose I/O Pins

| Signal      | Type | Name/Description  |
|-------------|------|---|
| CCLKDS      | I    | <b>Common Clock Downstream.</b> When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.  |
| CCLKUS      | I    | <b>Common Clock Upstream.</b> When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.  |
| MSMBSMODE   | I    | <b>Master SMBus Slow Mode.</b> The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.  |
| PENTBRSTN   | I    | <b>Non-Transparent Bridge Reset.</b> Assertion of this signal indicates a reset on the external side of the non-transparent bridge. This signal is only used when the switch mode selects a non-transparent mode and has no effect otherwise.   |
| PERSTN      | I    | <b>Fundamental Reset.</b> Assertion of this signal resets all logic inside the PES12NT3 and initiates a PCI Express fundamental reset.  |
| RSTHALT     | I    | <b>Reset Halt.</b> When this signal is asserted during a PCI Express fundamental reset, the PES12NT3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master. |
| SWMODE[3:0] | I    | <b>Switch Mode.</b> These configuration pins determine the PES12NT3 switch operating mode.<br>0x0 - Reserved<br>0x1 - Reserved<br>0x2 - Non-transparent mode<br>0x3 - Non-transparent mode with serial EEPROM initialization<br>0x4 - Non-transparent failover mode<br>0x5 - Non-transparent failover mode with serial EEPROM initialization<br>0x6 through 0xF - Reserved  |

Table 4 System Pins

| Signal   | Type | Name/Description  |
|----------|------|---|
| JTAG_TCK | I    | <b>JTAG Clock.</b> This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle. |
| JTAG_TDI | I    | <b>JTAG Data Input.</b> This is the serial data input to the boundary scan logic or JTAG Controller.  |

Table 5 Test Pins (Part 1 of 2)

| Signal      | Type | Name/Description   |
|-------------|------|--|
| JTAG_TDO    | O    | <b>JTAG Data Output.</b> This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.  |
| JTAG_TMS    | I    | <b>JTAG Mode.</b> The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.  |
| JTAG_TRST_N | I    | <b>JTAG Reset.</b> This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur:<br>1) actively drive this signal low with control logic<br>2) statically drive this signal low with an external pull-down on the board |

Table 5 Test Pins (Part 2 of 2)

| Signal               | Type | Name/Description   |
|----------------------|------|--|
| V <sub>DD</sub> CORE | I    | <b>Core V<sub>DD</sub>.</b> Power supply for core logic.   |
| V <sub>DD</sub> IO   | I    | <b>I/O V<sub>DD</sub>.</b> LVTTTL I/O buffer power supply.   |
| V <sub>DD</sub> PE   | I    | <b>PCI Express Digital Power.</b> PCI Express digital power used by the digital power of the SerDes. |
| V <sub>DD</sub> APE  | I    | <b>PCI Express Analog Power.</b> PCI Express analog power used by the PLL and bias generator.        |
| V <sub>TT</sub> PE   | I    | <b>PCI Express Termination Power.</b>  |
| V <sub>SS</sub>      | I    | Ground.  |

Table 6 Power and Ground Pins

## Pin Characteristics

**Note:** Some input pads of the PES12NT3 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

| Function              | Pin Name        | Type           | Buffer | I/O Type             | Internal Resistor    | Notes |
|-----------------------|-----------------|----------------|--------|----------------------|----------------------|-------|
| PCI Express Interface | PEALREV         | I              | LVTTTL | Input                | pull-down            |       |
|                       | PEARN[3:0]      | I              | CML    | Serial link          |                      |       |
|                       | PEARP[3:0]      | I              |        |                      |                      |       |
|                       | PEATN[3:0]      | O              |        |                      |                      |       |
|                       | PEATP[3:0]      | O              |        |                      |                      |       |
|                       | PEBLREV         | I              | LVTTTL | Input                | pull-down            |       |
|                       | PEBRN[3:0]      | I              | CML    | Serial link          |                      |       |
|                       | PEBRP[3:0]      | I              |        |                      |                      |       |
|                       | PEBTN[3:0]      | O              |        |                      |                      |       |
|                       | PEBTP[3:0]      | O              |        |                      |                      |       |
|                       | PECLREV         | I              | LVTTTL | Input                | pull-down            |       |
|                       | PECRN[3:0]      | I              | CML    | Serial link          |                      |       |
|                       | PECRP[3:0]      | I              |        |                      |                      |       |
|                       | PECTN[3:0]      | O              |        |                      |                      |       |
|                       | PECTP[3:0]      | O              |        |                      |                      |       |
|                       |                 | PEREFCLKN[1:0] | I      | LVPECL/<br>CML       | Diff. Clock<br>Input |       |
|                       | PEREFCLKP[1:0]  | I              |        |                      |                      |       |
|                       | REFCLKM         | I              | LVTTTL | Input                | pull-down            |       |
| SMBus                 | MSMBADDR[4:1]   | I              | LVTTTL | Input                | pull-up              |       |
|                       | MSMBCLK         | I/O            |        | STI                  |                      |       |
|                       | MSMBDAT         | I/O            |        |                      |                      |       |
|                       | SSMBADDR[5,3:1] | I              |        | Input                | pull-up              |       |
|                       | SSMBCLK         | I/O            |        | STI                  |                      |       |
|                       | SSMBDAT         | I/O            |        |                      |                      |       |
| General Purpose I/O   | GPIO[7:0]       | I/O            | LVTTTL | Input,<br>High Drive | pull-up              |       |

Table 7 Pin Characteristics (Part 1 of 2)



| Function    | Pin Name    | Type | Buffer | I/O Type  | Internal Resistor | Notes              |
|-------------|-------------|------|--------|-----------|-------------------|--------------------|
| System Pins | CCLKDS      | I    | LVTTL  | Input     | pull-up           |                    |
|             | CCLKUS      | I    |        |           | pull-up           |                    |
|             | MSMBSMODE   | I    |        |           | pull-down         |                    |
|             | PENTBRSTN   | I    |        |           |                   |                    |
|             | PERSTN      | I    |        |           |                   |                    |
|             | RSTHALT     | I    |        |           | pull-down         |                    |
|             | SWMODE[3:0] | I    |        |           | pull-up           |                    |
| JTAG        | JTAG_TCK    | I    | LVTTL  | STI       | pull-up           |                    |
|             | JTAG_TDI    | I    |        |           | pull-up           |                    |
|             | JTAG_TDO    | O    |        | Low Drive |                   |                    |
|             | JTAG_TMS    | I    |        | STI       | pull-up           |                    |
|             | JTAG_TRST_N | I    |        |           | pull-up           | External pull-down |

Table 7 Pin Characteristics (Part 2 of 2)

# Logic Diagram — PES12NT3

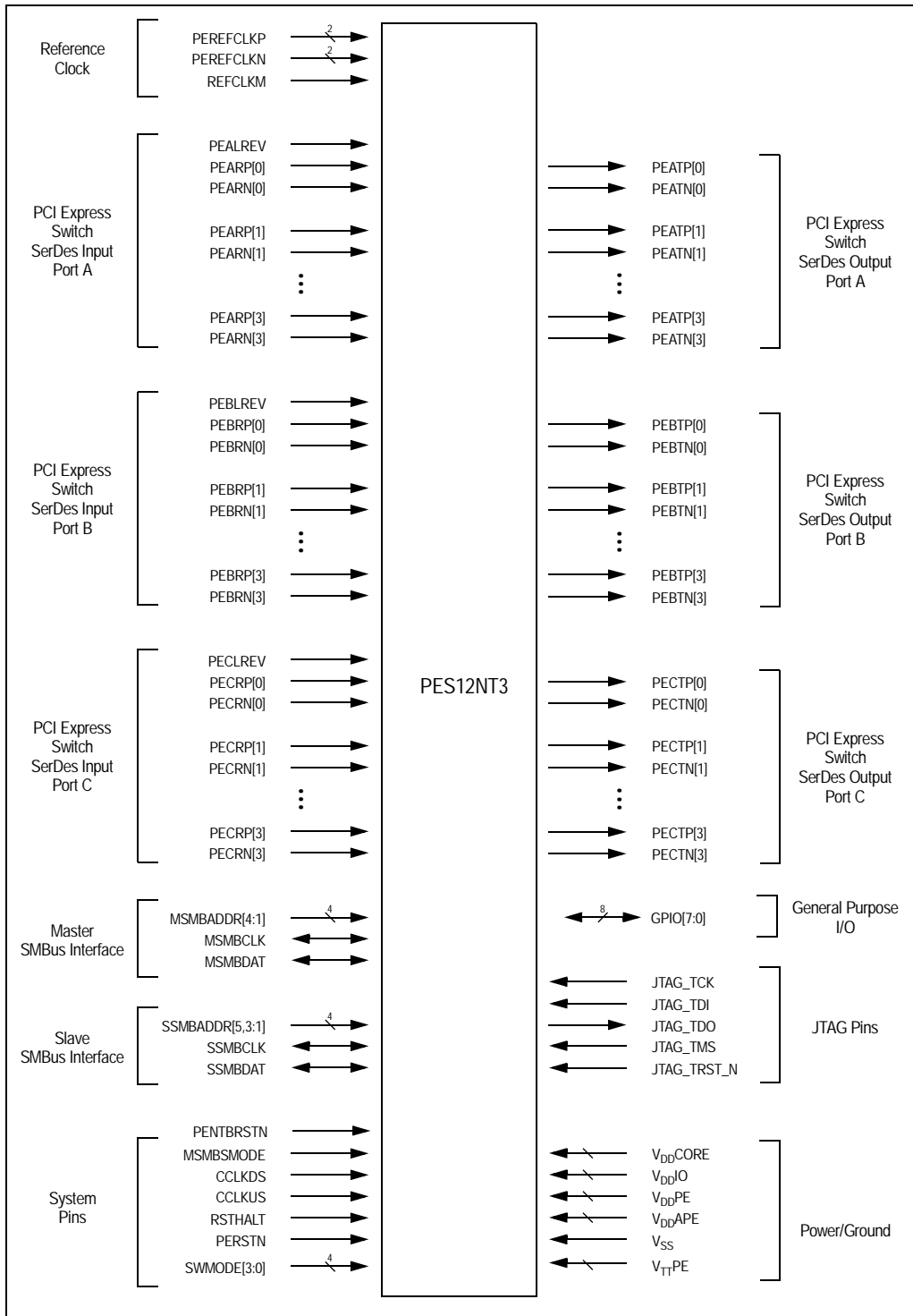


Figure 4 PES12NT3 Logic Diagram

## System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

| Parameter                         | Description                                   | Min | Typical | Max              | Unit              |
|-----------------------------------|---|-----|---------|------------------|-------------------|
| Refclk <sub>FREQ</sub>            | Input reference clock frequency range         | 100 |         | 125 <sup>1</sup> | MHz               |
| Refclk <sub>DC</sub> <sup>2</sup> | Duty cycle of input clock                     | 40  | 50      | 60               | %                 |
| T <sub>R</sub> , T <sub>F</sub>   | Rise/Fall time of input clocks                |     |         | 0.2*RCUI         | RCUI <sup>3</sup> |
| V <sub>SW</sub>                   | Differential input voltage swing <sup>4</sup> | 0.6 |         | 1.6              | V                 |
| T <sub>jitter</sub>               | Input clock jitter (cycle-to-cycle)           |     |         | 125              | ps                |

**Table 8 Input Clock Requirements**

<sup>1</sup> The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.

<sup>2</sup> ClkIn must be AC coupled. Use 0.01 — 0.1 μF ceramic capacitors.

<sup>3</sup> RCUI (Reference Clock Unit Interval) refers to the reference clock period.

<sup>4</sup> AC coupling required.

## AC Timing Characteristics

| Parameter                                   | Description  | Min <sup>1</sup> | Typical <sup>1</sup> | Max <sup>1</sup> | Units |
|---|--|------------------|----------------------|------------------|-------|
| <b>PCIe Transmit</b>                        |  |                  |                      |                  |       |
| UI  | Unit Interval  | 399.88           | 400                  | 400.12           | ps    |
| T <sub>TX-EYE</sub>                         | Minimum Tx Eye Width   | 0.7              | .9                   |                  | UI    |
| T <sub>TX-EYE-MEDIAN-to-MAX-JITTER</sub>    | Maximum time between the jitter median and maximum deviation from the median |                  |                      | 0.15             | UI    |
| T <sub>TX-RISE</sub> , T <sub>TX-FALL</sub> | D+ / D- Tx output rise/fall time   | 50               | 90                   |                  | ps    |
| T <sub>TX-IDLE-MIN</sub>                    | Minimum time in idle   | 50               |                      |                  | UI    |
| T <sub>TX-IDLE-SET-TO-IDLE</sub>            | Maximum time to transition to a valid Idle after sending an Idle ordered set |                  |                      | 20               | UI    |
| T <sub>TX-IDLE-TO-DIFF-DATA</sub>           | Maximum time to transition from valid idle to diff data                      |                  |                      | 20               | UI    |
| T <sub>TX-IDLE-RCV-DET-MAX</sub>            | Max time spend in idle before initiating a RX detect sequence                |                  | 20                   | 100              | ms    |
| T <sub>TX-SKEW</sub>                        | Transmitter data skew between any 2 lanes                                    |                  | 500                  | 1300             | ps    |
| <b>PCIe Receive</b>                         |  |                  |                      |                  |       |
| UI  | Unit Interval  | 399.88           | 400                  | 400.12           | ps    |
| T <sub>RX-EYE (with jitter)</sub>           | Minimum Receiver Eye Width (jitter tolerance)                                | 0.4              |                      |                  | UI    |

**Table 9 PCIe AC Timing Characteristics (Part 1 of 2)**

| Parameter                                | Description   | Min <sup>1</sup> | Typical <sup>1</sup> | Max <sup>1</sup> | Units |
|--|---|------------------|----------------------|------------------|-------|
| T <sub>RX-EYE-MEDIUM TO MAX JITTER</sub> | Max time between jitter median & max deviation          |                  |                      | 0.3              | UI    |
| T <sub>RX-IDLE-DET-DIFF-ENTER TIME</sub> | Unexpected Idle Enter Detect Threshold Integration Time |                  |                      | 10               | ms    |
| T <sub>RX-SKEW</sub>                     | Lane to lane input skew                                 |                  |                      | 20               | ns    |

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

<sup>1</sup> Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a

| Signal                 | Symbol               | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|------------------------|----------------------|----------------|-----|-----|------|--------------------------|
| <b>GPIO</b>            |                      |                |     |     |      |                          |
| GPIO[7:0] <sup>1</sup> | Tpw_13b <sup>2</sup> | None           | 50  | —   | ns   |                          |

Table 10 GPIO AC Timing Characteristics

<sup>1</sup> GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

<sup>2</sup> The values for this symbol were determined by calculation, not by testing.

| Signal                           | Symbol               | Reference Edge   | Min  | Max  | Unit | Timing Diagram Reference |
|----------------------------------|----------------------|------------------|------|------|------|--------------------------|
| <b>JTAG</b>                      |                      |                  |      |      |      |                          |
| JTAG_TCK                         | Tper_16a             | none             | 50.0 | —    | ns   | See Figure 5.            |
|                                  | Thigh_16a, Tlow_16a  |                  | 10.0 | 25.0 | ns   |                          |
| JTAG_TMS <sup>1</sup> , JTAG_TDI | Tsu_16b              | JTAG_TCK rising  | 2.4  | —    | ns   |                          |
|                                  | Thld_16b             |                  | 1.0  | —    | ns   |                          |
| JTAG_TDO                         | Tdo_16c              | JTAG_TCK falling | —    | 20   | ns   |                          |
|                                  | Tdz_16c <sup>2</sup> |                  | —    | 20   | ns   |                          |
| JTAG_TRST_N                      | Tpw_16d <sup>2</sup> | none             | 25.0 | —    | ns   |                          |

Table 11 JTAG AC Timing Characteristics

<sup>1</sup> The JTAG specification, IEEE 1149.1, recommends that JTAG\_TMS should be held at 1 while the signal applied at JTAG\_TRST\_N changes from 0 to 1. Otherwise, a race may occur if JTAG\_TRST\_N is deasserted (going from low to high) on a rising edge of JTAG\_TCK when JTAG\_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

<sup>2</sup> The values for this symbol were determined by calculation, not by testing.

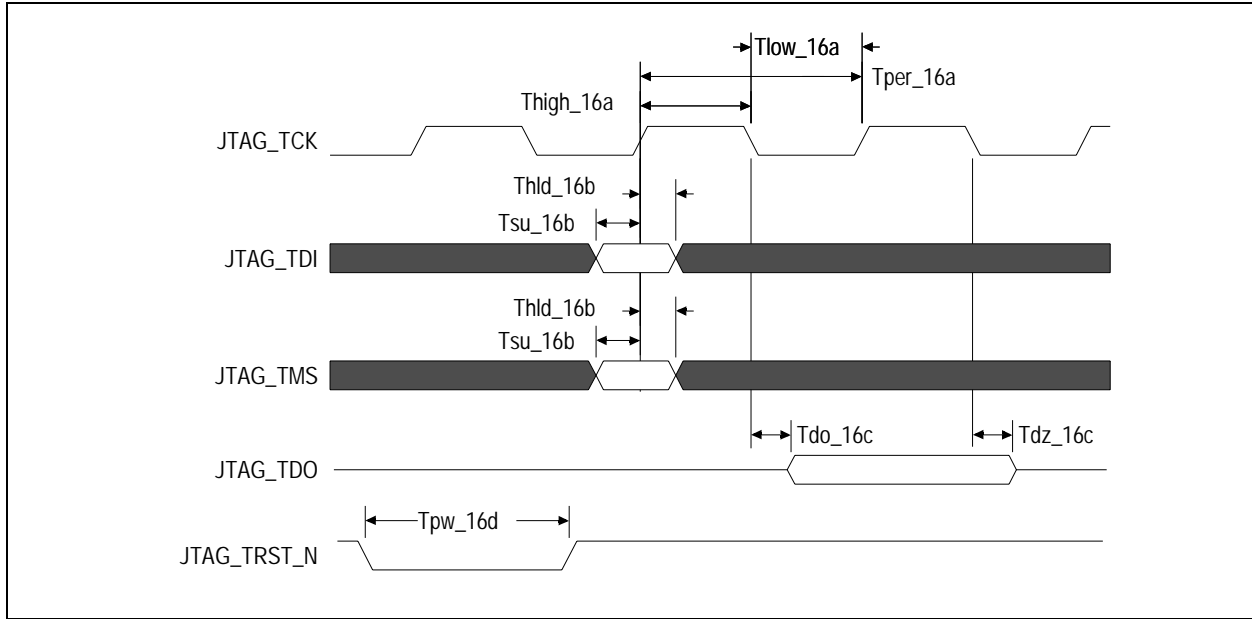


Figure 5 JTAG AC Timing Waveform

## Recommended Operating Supply Voltages

| Symbol               | Parameter  | Minimum | Typical | Maximum | Unit |
|----------------------|--|---------|---------|---------|------|
| V <sub>DD</sub> CORE | Internal logic supply                                | 0.9     | 1.0     | 1.1     | V    |
| V <sub>DD</sub> I/O  | I/O supply except for SerDes LVPECL/CML              | 3.0     | 3.3     | 3.6     | V    |
| V <sub>DD</sub> PE   | PCI Express Digital Power                            | 0.9     | 1.0     | 1.1     | V    |
| V <sub>DD</sub> APE  | PCI Express Analog Power                             | 0.9     | 1.0     | 1.1     | V    |
| V <sub>TT</sub> PE   | PCI Express Serial Data Transmit Termination Voltage | 1.425   | 1.5     | 1.575   | V    |
| V <sub>SS</sub>      | Common ground  | 0       | 0       | 0       | V    |

Table 12 PES12NT3 Operating Voltages

## Recommended Operating Temperature

| Grade      | Temperature          |
|------------|----------------------|
| Commercial | 0°C to +70°C Ambient |

Table 13 PES12NT3 Operating Temperatures

## Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES12NT3, the power-up sequence must be as follows:

1.  $V_{DD}I/O$  — 3.3V
2.  $V_{DD}Core$ ,  $V_{DD}PE$ ,  $V_{DD}APE$  — 1.0V
3.  $V_{TT}PE$  — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

## Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

| Number of Connected Lanes:<br>Port-A/Port-B/Port-C | Core (Watts)<br>(1.0V supply) |      | PCIe Digital<br>(Watts)<br>(1.0V supply) |      | PCIe Analog<br>(Watts)<br>(1.0V supply) |      | PCIe Termin-<br>ation (Watts)<br>(1.5V supply) |      | I/O (Watts)<br>(3.3V supply) |      | Total (Watts) |      |
|--|-------------------------------|------|--|------|---|------|--|------|------------------------------|------|---------------|------|
|  | Typ                           | Max  | Typ                                      | Max  | Typ                                     | Max  | Typ  | Max  | Typ                          | Max  | Typ           | Max  |
| 1/1/1  | 0.52                          | 0.67 | 0.27                                     | 0.36 | 0.13                                    | 0.16 | 0.11   | 0.13 | 0.01                         | 0.01 | 1.04          | 1.33 |
| 4/1/1  | 0.56                          | 0.76 | 0.47                                     | 0.58 | 0.19                                    | 0.21 | 0.22   | 0.26 | 0.01                         | 0.01 | 1.44          | 1.81 |
| 4/4/4  | 0.65                          | 0.89 | 0.68                                     | 0.81 | 0.21                                    | 0.25 | 0.38   | 0.51 | 0.01                         | 0.01 | 1.92          | 2.47 |

Table 14 PES12NT3 Power Consumption

## DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

| I/O Type                         | Parameter                                     | Description   | Min <sup>1</sup> | Typ <sup>1</sup> | Max <sup>1</sup> | Unit | Conditions |
|----------------------------------|---|---|------------------|------------------|------------------|------|------------|
| Serial Link                      | <b>PCIe Transmit</b>                          |   |                  |                  |                  |      |            |
|                                  | V <sub>TX-DIFFp-p</sub>                       | Differential peak-to-peak output voltage                | 800              |                  | 1200             | mV   |            |
|                                  | V <sub>TX-DE-RATIO</sub>                      | De-emphasized differential output voltage               | -3               |                  | -4               | dB   |            |
|                                  | V <sub>TX-DC-CM</sub>                         | DC Common mode voltage                                  | -0.1             | 1                | 3.7              | V    |            |
|                                  | V <sub>TX-CM-ACP</sub>                        | RMS AC peak common mode output voltage                  |                  |                  | 20               | mV   |            |
|                                  | V <sub>TX-CM-DC-active-idle-delta</sub>       | Abs delta of DC common mode voltage between L0 and idle |                  |                  | 100              | mV   |            |
|                                  | V <sub>TX-CM-DC-line-delta</sub>              | Abs delta of DC common mode voltage between D+ and D-   |                  |                  | 25               | mV   |            |
|                                  | V <sub>TX-Idle-DiffP</sub>                    | Electrical idle diff peak output                        |                  |                  | 20               | mV   |            |
|                                  | V <sub>TX-RCV-Detect</sub>                    | Voltage change during receiver detection                |                  |                  | 600              | mV   |            |
|                                  | RL <sub>TX-DIFF</sub>                         | Transmitter Differential Return loss                    | 12               |                  |                  | dB   |            |
|                                  | RL <sub>TX-CM</sub>                           | Transmitter Common Mode Return loss                     | 6                |                  |                  | dB   |            |
|                                  | Z <sub>TX-DEFF-DC</sub>                       | DC Differential TX impedance                            | 80               | 100              | 120              | Ω    |            |
|                                  | Z <sub>OSE</sub>                              | Single ended TX Impedance                               | 40               | 50               | 60               | Ω    |            |
|                                  | Transmitter Eye Diagram                       | TX Eye Height (De-emphasized bits)                      | 505              | 650              |                  | mV   |            |
|                                  | Transmitter Eye Diagram                       | TX Eye Height (Transition bits)                         | 800              | 950              |                  | mV   |            |
|                                  | <b>PCIe Receive</b>                           |   |                  |                  |                  |      |            |
|                                  | V <sub>RX-DIFFp-p</sub>                       | Differential input voltage (peak-to-peak)               | 175              |                  | 1200             | mV   |            |
|                                  | V <sub>RX-CM-AC</sub>                         | Receiver common-mode voltage for AC coupling            |                  |                  | 150              | mV   |            |
|                                  | RL <sub>RX-DIFF</sub>                         | Receiver Differential Return Loss                       | 15               |                  |                  | dB   |            |
|                                  | RL <sub>RX-CM</sub>                           | Receiver Common Mode Return Loss                        | 6                |                  |                  | dB   |            |
| Z <sub>RX-DIFF-DC</sub>          | Differential input impedance (DC)             | 80  | 100              | 120              | Ω                |      |            |
| Z <sub>RX-COMM-DC</sub>          | Single-ended input impedance                  | 40  | 50               | 60               | Ω                |      |            |
| Z <sub>RX-COMM-HIGH-Z-DC</sub>   | Powered down input common mode impedance (DC) | 200k  | 350k             |                  | Ω                |      |            |
| V <sub>RX-IDLE-DET-DIFFp-p</sub> | Electrical idle detect threshold              | 65  |                  | 175              | mV               |      |            |
| <b>PCIe REFCLK</b>               |   |   |                  |                  |                  |      |            |
|                                  | C <sub>IN</sub>                               | Input Capacitance                                       | 1.5              | —                |                  | pF   |            |

Table 15 DC Electrical Characteristics (Part 1 of 2)

| I/O Type                    | Parameter                               | Description | Min <sup>1</sup> | Typ <sup>1</sup> | Max <sup>1</sup>          | Unit | Conditions                |
|-----------------------------|---|-------------|------------------|------------------|---------------------------|------|---------------------------|
| <b>Other I/Os</b>           |   |             |                  |                  |                           |      |                           |
| LOW Drive Output            | I <sub>OL</sub>                         |             | —                | 2.5              | —                         | mA   | V <sub>OL</sub> = 0.4v    |
|                             | I <sub>OH</sub>                         |             | —                | -5.5             | —                         | mA   | V <sub>OH</sub> = 1.5V    |
| High Drive Output           | I <sub>OL</sub>                         |             | —                | 12.0             | —                         | mA   | V <sub>OL</sub> = 0.4v    |
|                             | I <sub>OH</sub>                         |             | —                | -20.0            | —                         | mA   | V <sub>OH</sub> = 1.5V    |
| Schmitt Trigger Input (STI) | V <sub>IL</sub>                         |             | -0.3             | —                | 0.8                       | V    | —                         |
|                             | V <sub>IH</sub>                         |             | 2.0              | —                | V <sub>DD</sub> I/O + 0.5 | V    | —                         |
| Input                       | V <sub>IL</sub>                         |             | -0.3             | —                | 0.8                       | V    | —                         |
|                             | V <sub>IH</sub>                         |             | 2.0              | —                | V <sub>DD</sub> I/O + 0.5 | V    | —                         |
| Capacitance                 | C <sub>IN</sub>                         |             | —                | —                | 8.5                       | pF   | —                         |
| Leakage                     | Inputs                                  |             | —                | —                | ± 10                      | μA   | V <sub>DD</sub> I/O (max) |
|                             | I/O <sub>LEAK</sub> w/o Pull-ups/downs  |             | —                | —                | ± 10                      | μA   | V <sub>DD</sub> I/O (max) |
|                             | I/O <sub>LEAK</sub> WITH Pull-ups/downs |             | —                | —                | ± 80                      | μA   | V <sub>DD</sub> I/O (max) |

Table 15 DC Electrical Characteristics (Part 2 of 2)

<sup>1</sup>: Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.



## Package Pinout — 324-BGA Signal Pinout for PES12NT3

The following table lists the pin numbers and signal names for the PES12NT3 device.

| Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| A1  | V <sub>SS</sub>      |     | E10 | V <sub>DD</sub> PE   |     | K1  | V <sub>DD</sub> CORE |     | P10 | V <sub>DD</sub> IO   |     |
| A2  | V <sub>SS</sub>      |     | E11 | V <sub>SS</sub>      |     | K2  | V <sub>SS</sub>      |     | P11 | V <sub>DD</sub> IO   |     |
| A3  | PEARP03              |     | E12 | V <sub>DD</sub> PE   |     | K3  | V <sub>TT</sub> PE   |     | P12 | V <sub>DD</sub> IO   |     |
| A4  | V <sub>DD</sub> CORE |     | E13 | V <sub>SS</sub>      |     | K4  | V <sub>DD</sub> CORE |     | P13 | V <sub>DD</sub> IO   |     |
| A5  | PEATN03              |     | E14 | V <sub>DD</sub> CORE |     | K5  | V <sub>DD</sub> PE   |     | P14 | V <sub>DD</sub> IO   |     |
| A6  | V <sub>DD</sub> CORE |     | E15 | V <sub>DD</sub> APE  |     | K6  | V <sub>SS</sub>      |     | P15 | V <sub>SS</sub>      |     |
| A7  | PEATP02              |     | E16 | V <sub>SS</sub>      |     | K7  | V <sub>SS</sub>      |     | P16 | V <sub>TT</sub> PE   |     |
| A8  | V <sub>DD</sub> CORE |     | E17 | PECTP03              |     | K8  | V <sub>SS</sub>      |     | P17 | V <sub>SS</sub>      |     |
| A9  | PEARNO2              |     | E18 | PECTN03              |     | K9  | V <sub>SS</sub>      |     | P18 | V <sub>DD</sub> CORE |     |
| A10 | V <sub>DD</sub> CORE |     | F1  | V <sub>DD</sub> CORE |     | K10 | V <sub>SS</sub>      |     | R1  | PEBTN03              |     |
| A11 | PEARP01              |     | F2  | V <sub>SS</sub>      |     | K11 | V <sub>SS</sub>      |     | R2  | PEBTP03              |     |
| A12 | V <sub>DD</sub> CORE |     | F3  | V <sub>DD</sub> CORE |     | K12 | V <sub>SS</sub>      |     | R3  | V <sub>SS</sub>      |     |
| A13 | PEATP01              |     | F4  | V <sub>DD</sub> APE  |     | K13 | V <sub>SS</sub>      |     | R4  | V <sub>DD</sub> IO   |     |
| A14 | V <sub>DD</sub> CORE |     | F5  | V <sub>SS</sub>      |     | K14 | V <sub>SS</sub>      |     | R5  | V <sub>SS</sub>      |     |
| A15 | V <sub>DD</sub> CORE |     | F6  | V <sub>DD</sub> CORE |     | K15 | V <sub>DD</sub> PE   |     | R6  | V <sub>DD</sub> CORE |     |
| A16 | PEATN00              |     | F7  | V <sub>SS</sub>      |     | K16 | V <sub>TT</sub> PE   |     | R7  | MSMBDAT              |     |
| A17 | V <sub>SS</sub>      |     | F8  | V <sub>DD</sub> CORE |     | K17 | V <sub>SS</sub>      |     | R8  | SSMBADDR_5           |     |
| A18 | V <sub>SS</sub>      |     | F9  | V <sub>SS</sub>      |     | K18 | V <sub>DD</sub> CORE |     | R9  | PEALREV              |     |
| B1  | V <sub>DD</sub> CORE |     | F10 | V <sub>DD</sub> CORE |     | L1  | PEBRN02              |     | R10 | SWMODE_2             |     |
| B2  | V <sub>DD</sub> CORE |     | F11 | V <sub>SS</sub>      |     | L2  | PEBRP02              |     | R11 | RSTHALT              |     |
| B3  | PEARNO3              |     | F12 | V <sub>SS</sub>      |     | L3  | V <sub>SS</sub>      |     | R12 | GPIO_04              | 1   |
| B4  | V <sub>SS</sub>      |     | F13 | V <sub>DD</sub> PE   |     | L4  | V <sub>DD</sub> PE   |     | R13 | V <sub>DD</sub> CORE |     |
| B5  | PEATP03              |     | F14 | V <sub>SS</sub>      |     | L5  | V <sub>SS</sub>      |     | R14 | V <sub>SS</sub>      |     |
| B6  | V <sub>SS</sub>      |     | F15 | V <sub>DD</sub> IO   |     | L6  | V <sub>DD</sub> CORE |     | R15 | V <sub>DD</sub> IO   |     |
| B7  | PEATN02              |     | F16 | V <sub>SS</sub>      |     | L7  | V <sub>DD</sub> CORE |     | R16 | V <sub>SS</sub>      |     |
| B8  | V <sub>SS</sub>      |     | F17 | V <sub>SS</sub>      |     | L8  | V <sub>DD</sub> CORE |     | R17 | PECTP00              |     |
| B9  | PEARP02              |     | F18 | V <sub>DD</sub> CORE |     | L9  | V <sub>DD</sub> CORE |     | R18 | PECTN00              |     |
| B10 | V <sub>SS</sub>      |     | G1  | PEBTP01              |     | L10 | V <sub>DD</sub> CORE |     | T1  | V <sub>DD</sub> CORE |     |
| B11 | PEARNO1              |     | G2  | PEBTN01              |     | L11 | V <sub>DD</sub> CORE |     | T2  | V <sub>SS</sub>      |     |
| B12 | V <sub>SS</sub>      |     | G3  | V <sub>SS</sub>      |     | L12 | V <sub>DD</sub> CORE |     | T3  | V <sub>SS</sub>      |     |
| B13 | PEATN01              |     | G4  | V <sub>DD</sub> PE   |     | L13 | V <sub>DD</sub> CORE |     | T4  | JTAG_TCK             |     |
| B14 | V <sub>SS</sub>      |     | G5  | V <sub>DD</sub> APE  |     | L14 | V <sub>SS</sub>      |     | T5  | JTAG_TDO             |     |
| B15 | V <sub>SS</sub>      |     | G6  | V <sub>SS</sub>      |     | L15 | V <sub>DD</sub> PE   |     | T6  | MSMBADDR_1           |     |
| B16 | PEATP00              |     | G7  | V <sub>SS</sub>      |     | L16 | V <sub>SS</sub>      |     | T7  | MSMBCLK              |     |

Table 16 PES12NT3 324-pin Signal Pin-Out (Part 1 of 3)

| Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| B17 | V <sub>DD</sub> CORE |     | G8  | V <sub>DD</sub> IO   |     | L17 | PECRP01              |     | T8  | SSMBADDR_2           |     |
| B18 | V <sub>DD</sub> CORE |     | G9  | V <sub>SS</sub>      |     | L18 | PECRN01              |     | T9  | CCLKDS               |     |
| C1  | PEBRP00              |     | G10 | V <sub>DD</sub> IO   |     | M1  | V <sub>DD</sub> CORE |     | T10 | SWMODE_1             |     |
| C2  | PEBRN00              |     | G11 | V <sub>SS</sub>      |     | M2  | V <sub>SS</sub>      |     | T11 | PERSTN               |     |
| C3  | V <sub>SS</sub>      |     | G12 | V <sub>DD</sub> CORE |     | M3  | V <sub>SS</sub>      |     | T12 | GPIO_03              | 1   |
| C4  | V <sub>DD</sub> CORE |     | G13 | V <sub>SS</sub>      |     | M4  | V <sub>DD</sub> APE  |     | T13 | GPIO_07              |     |
| C5  | V <sub>SS</sub>      |     | G14 | V <sub>DD</sub> APE  |     | M5  | V <sub>SS</sub>      |     | T14 | V <sub>SS</sub>      |     |
| C6  | V <sub>TT</sub> PE   |     | G15 | V <sub>DD</sub> PE   |     | M6  | V <sub>DD</sub> CORE |     | T15 | REFCLKM              |     |
| C7  | V <sub>SS</sub>      |     | G16 | V <sub>SS</sub>      |     | M7  | V <sub>SS</sub>      |     | T16 | V <sub>SS</sub>      |     |
| C8  | V <sub>TT</sub> PE   |     | G17 | PECTN02              |     | M8  | V <sub>SS</sub>      |     | T17 | V <sub>SS</sub>      |     |
| C9  | V <sub>SS</sub>      |     | G18 | PECTP02              |     | M9  | V <sub>DD</sub> CORE |     | T18 | V <sub>DD</sub> CORE |     |
| C10 | V <sub>TT</sub> PE   |     | H1  | V <sub>DD</sub> CORE |     | M10 | V <sub>DD</sub> CORE |     | U1  | PEBRP03              |     |
| C11 | V <sub>SS</sub>      |     | H2  | V <sub>SS</sub>      |     | M11 | V <sub>SS</sub>      |     | U2  | PEBRN03              |     |
| C12 | V <sub>TT</sub> PE   |     | H3  | V <sub>TT</sub> PE   |     | M12 | V <sub>SS</sub>      |     | U3  | V <sub>SS</sub>      |     |
| C13 | V <sub>DD</sub> CORE |     | H4  | V <sub>DD</sub> APE  |     | M13 | V <sub>DD</sub> CORE |     | U4  | JTAG_TDI             |     |
| C14 | PEARP00              |     | H5  | V <sub>SS</sub>      |     | M14 | V <sub>SS</sub>      |     | U5  | JTAG_TMS             |     |
| C15 | PEARN00              |     | H6  | V <sub>SS</sub>      |     | M15 | V <sub>DD</sub> APE  |     | U6  | MSMBADDR_2           |     |
| C16 | V <sub>DD</sub> CORE |     | H7  | V <sub>DD</sub> CORE |     | M16 | V <sub>SS</sub>      |     | U7  | MSMBADDR_4           |     |
| C17 | PECRN03              |     | H8  | V <sub>SS</sub>      |     | M17 | V <sub>SS</sub>      |     | U8  | SSMBADDR_3           |     |
| C18 | PECRP03              |     | H9  | V <sub>DD</sub> CORE |     | M18 | V <sub>DD</sub> CORE |     | U9  | CCLKUS               |     |
| D1  | V <sub>DD</sub> CORE |     | H10 | V <sub>DD</sub> CORE |     | N1  | PEBTP02              |     | U10 | SWMODE_0             |     |
| D2  | V <sub>SS</sub>      |     | H11 | V <sub>SS</sub>      |     | N2  | PEBTN02              |     | U11 | PECLREV              |     |
| D3  | V <sub>SS</sub>      |     | H12 | V <sub>DD</sub> CORE |     | N3  | V <sub>TT</sub> PE   |     | U12 | GPIO_00              |     |
| D4  | V <sub>DD</sub> CORE |     | H13 | V <sub>SS</sub>      |     | N4  | V <sub>DD</sub> APE  |     | U13 | GPIO_02              | 1   |
| D5  | V <sub>SS</sub>      |     | H14 | V <sub>DD</sub> APE  |     | N5  | V <sub>SS</sub>      |     | U14 | GPIO_06              |     |
| D6  | V <sub>DD</sub> APE  |     | H15 | V <sub>DD</sub> PE   |     | N6  | V <sub>SS</sub>      |     | U15 | MSMBSMODE            |     |
| D7  | V <sub>SS</sub>      |     | H16 | V <sub>TT</sub> PE   |     | N7  | V <sub>SS</sub>      |     | U16 | V <sub>SS</sub>      |     |
| D8  | V <sub>DD</sub> APE  |     | H17 | V <sub>SS</sub>      |     | N8  | V <sub>SS</sub>      |     | U17 | PECRN00              |     |
| D9  | V <sub>SS</sub>      |     | H18 | V <sub>DD</sub> CORE |     | N9  | V <sub>SS</sub>      |     | U18 | PECRP00              |     |
| D10 | V <sub>DD</sub> APE  |     | J1  | PEBRP01              |     | N10 | V <sub>SS</sub>      |     | V1  | V <sub>DD</sub> CORE |     |
| D11 | V <sub>SS</sub>      |     | J2  | PEBRN01              |     | N11 | V <sub>SS</sub>      |     | V2  | V <sub>SS</sub>      |     |
| D12 | V <sub>DD</sub> APE  |     | J3  | V <sub>SS</sub>      |     | N12 | V <sub>SS</sub>      |     | V3  | PEREFCLKP1           |     |
| D13 | V <sub>SS</sub>      |     | J4  | V <sub>DD</sub> PE   |     | N13 | V <sub>SS</sub>      |     | V4  | PEREFCLKN1           |     |
| D14 | V <sub>DD</sub> CORE |     | J5  | V <sub>SS</sub>      |     | N14 | V <sub>SS</sub>      |     | V5  | JTAG_TRST_N          |     |
| D15 | V <sub>SS</sub>      |     | J6  | V <sub>DD</sub> CORE |     | N15 | V <sub>DD</sub> APE  |     | V6  | MSMBADDR_3           |     |
| D16 | V <sub>SS</sub>      |     | J7  | V <sub>SS</sub>      |     | N16 | V <sub>TT</sub> PE   |     | V7  | SSMBADDR_1           |     |
| D17 | V <sub>SS</sub>      |     | J8  | V <sub>SS</sub>      |     | N17 | PECTN01              |     | V8  | SSMBCLK              |     |

Table 16 PES12NT3 324-pin Signal Pin-Out (Part 2 of 3)

| Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| D18 | V <sub>DD</sub> CORE |     | J9  | V <sub>DD</sub> CORE |     | N18 | PECTP01              |     | V9  | SSMBDAT              |     |
| E1  | PEBTN00              |     | J10 | V <sub>DD</sub> CORE |     | P1  | V <sub>DD</sub> CORE |     | V10 | PEBLREV              |     |
| E2  | PEBTP00              |     | J11 | V <sub>SS</sub>      |     | P2  | V <sub>SS</sub>      |     | V11 | SWMODE_3             |     |
| E3  | V <sub>DD</sub> CORE |     | J12 | V <sub>SS</sub>      |     | P3  | V <sub>TT</sub> PE   |     | V12 | PENTBRSTN            |     |
| E4  | V <sub>SS</sub>      |     | J13 | V <sub>DD</sub> CORE |     | P4  | V <sub>SS</sub>      |     | V13 | GPIO_01              |     |
| E5  | V <sub>DD</sub> CORE |     | J14 | V <sub>SS</sub>      |     | P5  | V <sub>DD</sub> IO   |     | V14 | GPIO_05              | 1   |
| E6  | V <sub>SS</sub>      |     | J15 | V <sub>DD</sub> CORE |     | P6  | V <sub>DD</sub> IO   |     | V15 | PEREFCLKP2           |     |
| E7  | V <sub>SS</sub>      |     | J16 | V <sub>SS</sub>      |     | P7  | V <sub>DD</sub> IO   |     | V16 | PEREFCLKN2           |     |
| E8  | V <sub>DD</sub> PE   |     | J17 | PECRP02              |     | P8  | V <sub>DD</sub> IO   |     | V17 | V <sub>SS</sub>      |     |
| E9  | V <sub>SS</sub>      |     | J18 | PECRN02              |     | P9  | V <sub>DD</sub> IO   |     | V18 | V <sub>DD</sub> CORE |     |

Table 16 PES12NT3 324-pin Signal Pin-Out (Part 3 of 3)

### Alternate Signal Functions

| Pin | GPIO    | Alternate |
|-----|---------|-----------|
| U13 | GPIO[2] | IOEXPINTN |
| T12 | GPIO[3] | PAABN     |
| R12 | GPIO[4] | PAAIN     |
| V14 | GPIO[5] | PAPIN     |

Table 17 PES12NT3 Alternate Signal Functions

## Power Pins

| V <sub>DD</sub> Core | V <sub>DD</sub> Core | V <sub>DD</sub> Core | V <sub>DD</sub> IO | V <sub>DD</sub> PE | V <sub>DD</sub> APE | V <sub>TT</sub> PE |
|----------------------|----------------------|----------------------|--------------------|--------------------|---------------------|--------------------|
| A4                   | F3                   | L8                   | F15                | E8                 | D6                  | C6                 |
| A6                   | F6                   | L9                   | G8                 | E10                | D8                  | C8                 |
| A8                   | F8                   | L10                  | G10                | E12                | D10                 | C10                |
| A10                  | F10                  | L11                  | P5                 | F13                | D12                 | C12                |
| A12                  | F18                  | L12                  | P6                 | G4                 | E15                 | H3                 |
| A14                  | G12                  | L13                  | P7                 | G15                | F4                  | H16                |
| A15                  | H1                   | M1                   | P8                 | H15                | G5                  | K3                 |
| B1                   | H7                   | M6                   | P9                 | J4                 | G14                 | K16                |
| B2                   | H9                   | M9                   | P10                | K5                 | H4                  | N3                 |
| B17                  | H10                  | M10                  | P11                | K15                | H14                 | N16                |
| B18                  | H12                  | M13                  | P12                | L4                 | M4                  | P3                 |
| C4                   | H18                  | M18                  | P13                | L15                | M15                 | P16                |
| C13                  | J6                   | P1                   | P14                |                    | N4                  |                    |
| C16                  | J9                   | P18                  | R4                 |                    | N15                 |                    |
| D1                   | J10                  | R6                   | R15                |                    |                     |                    |
| D4                   | J13                  | R13                  |                    |                    |                     |                    |
| D14                  | J15                  | T1                   |                    |                    |                     |                    |
| D18                  | K1                   | T18                  |                    |                    |                     |                    |
| E3                   | K4                   | V1                   |                    |                    |                     |                    |
| E5                   | K18                  | V18                  |                    |                    |                     |                    |
| E14                  | L6                   |                      |                    |                    |                     |                    |
| F1                   | L7                   |                      |                    |                    |                     |                    |

Table 18 PES12NT3 Power Pins

## Ground Pins

| V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> |
|-----------------|-----------------|-----------------|-----------------|-----------------|
| A1              | D16             | G16             | K13             | N12             |
| A2              | D17             | H2              | K14             | N13             |
| A17             | E4              | H5              | K17             | N14             |
| A18             | E6              | H6              | L3              | P2              |
| B4              | E7              | H8              | L5              | P4              |
| B6              | E9              | H11             | L14             | P15             |
| B8              | E11             | H13             | L16             | P17             |
| B10             | E13             | H17             | M2              | R3              |
| B12             | E16             | J3              | M3              | R5              |
| B14             | F2              | J5              | M5              | R14             |
| B15             | F5              | J7              | M7              | R16             |
| C3              | F7              | J8              | M8              | T2              |
| C5              | F9              | J11             | M11             | T3              |
| C7              | F11             | J12             | M12             | T14             |
| C9              | F12             | J14             | M14             | T16             |
| C11             | F14             | J16             | M16             | T17             |
| D2              | F16             | K2              | M17             | U3              |
| D3              | F17             | K6              | N5              | U16             |
| D5              | G3              | K7              | N6              | V2              |
| D7              | G6              | K8              | N7              | V17             |
| D9              | G7              | K9              | N8              |                 |
| D11             | G9              | K10             | N9              |                 |
| D13             | G11             | K11             | N10             |                 |
| D15             | G13             | K12             | N11             |                 |

Table 19 PES12NT3 Ground Pins

## Signals Listed Alphabetically

| Signal Name | I/O Type | Location | Signal Category              |
|-------------|----------|----------|------------------------------|
| CCLKDS      | I        | T9       | System                       |
| CCLKUS      | I        | U9       |                              |
| GPIO_00     | I/O      | U12      | General Purpose Input/Output |
| GPIO_01     | I/O      | V13      |                              |
| GPIO_02     | I/O      | U13      |                              |
| GPIO_03     | I/O      | T12      |                              |
| GPIO_04     | I/O      | R12      |                              |
| GPIO_05     | I/O      | V14      |                              |
| GPIO_06     | I/O      | U14      |                              |
| GPIO_07     | I/O      | T13      |                              |
| JTAG_TCK    | I        | T4       |                              |
| JTAG_TDI    | I        | U4       |                              |
| JTAG_TDO    | O        | T5       |                              |
| JTAG_TMS    | I        | U5       |                              |
| JTAG_TRST_N | I        | V5       |                              |
| MSMBADDR_1  | I        | T6       | SMBus                        |
| MSMBADDR_2  | I        | U6       |                              |
| MSMBADDR_3  | I        | V6       |                              |
| MSMBADDR_4  | I        | U7       |                              |
| MSMBCLK     | I/O      | T7       |                              |
| MSMBDAT     | I/O      | R7       |                              |
| MSMBSMODE   | I        | U15      | System                       |
| PEALREV     | I        | R9       | PCI Express                  |
| PEARN00     | I        | C15      |                              |
| PEARN01     | I        | B11      |                              |
| PEARN02     | I        | A9       |                              |
| PEARN03     | I        | B3       |                              |
| PEARP00     | I        | C14      |                              |
| PEARP01     | I        | A11      |                              |
| PEARP02     | I        | B9       |                              |
| PEARP03     | I        | A3       |                              |
| PEATN00     | O        | A16      |                              |
| PEATN01     | O        | B13      |                              |
| PEATN02     | O        | B7       |                              |

Table 20 PES12NT3 Alphabetical Signal List (Part 1 of 3)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|-----------------|
| PEATN03     | O        | A5       | PCI Express     |
| PEATP00     | O        | B16      |                 |
| PEATP01     | O        | A13      |                 |
| PEATP02     | O        | A7       |                 |
| PEATP03     | O        | B5       |                 |
| PEBLREV     | I        | V10      |                 |
| PEBRN00     | I        | C2       |                 |
| PEBRN01     | I        | J2       |                 |
| PEBRN02     | I        | L1       |                 |
| PEBRN03     | I        | U2       |                 |
| PEBRP00     | I        | C1       |                 |
| PEBRP01     | I        | J1       |                 |
| PEBRP02     | I        | L2       |                 |
| PEBRP03     | I        | U1       |                 |
| PEBTN00     | O        | E1       |                 |
| PEBTN01     | O        | G2       |                 |
| PEBTN02     | O        | N2       |                 |
| PEBTN03     | O        | R1       |                 |
| PEBTP00     | O        | E2       |                 |
| PEBTP01     | O        | G1       |                 |
| PEBTP02     | O        | N1       |                 |
| PEBTP03     | O        | R2       |                 |
| PECLREV     | I        | U11      |                 |
| PECRN00     | I        | U17      |                 |
| PECRN01     | I        | L18      |                 |
| PECRN02     | I        | J18      |                 |
| PECRN03     | I        | C17      |                 |
| PECRP00     | I        | U18      |                 |
| PECRP01     | I        | L17      |                 |
| PECRP02     | I        | J17      |                 |
| PECRP03     | I        | C18      |                 |
| PECTN00     | O        | R18      |                 |
| PECTN01     | O        | N17      |                 |
| PECTN02     | O        | G17      |                 |
| PECTN03     | O        | E18      |                 |
| PECTP00     | O        | R17      |                 |

Table 20 PES12NT3 Alphabetical Signal List (Part 2 of 3)

| Signal Name   | I/O Type                                   | Location | Signal Category |
|---|--|----------|-----------------|
| PECTP01   | O  | N18      | PCI Express     |
| PECTP02   | O  | G18      |                 |
| PECTP03   | O  | E17      |                 |
| PENTBRSTN   | I  | V12      | System          |
| PEREFCLKN1  | I  | V4       | PCI Express     |
| PEREFCLKN2  | I  | V16      |                 |
| PEREFCLKP1  | I  | V3       |                 |
| PEREFCLKP2  | I  | V15      |                 |
| PERSTN  | I  | T11      | System          |
| REFCLKM   | I  | T15      | PCI Express     |
| RSTHALT   | I  | R11      | System          |
| SSMBADDR_1  | I  | V7       | SMBus           |
| SSMBADDR_2  | I  | T8       |                 |
| SSMBADDR_3  | I  | U8       |                 |
| SSMBADDR_5  | I  | R8       |                 |
| SSMBCLK   | I/O  | V8       | SMBus           |
| SSMBDAT   | I/O  | V9       |                 |
| SWMODE_0  | I  | U10      | System          |
| SWMODE_1  | I  | T10      |                 |
| SWMODE_2  | I  | R10      |                 |
| SWMODE_3  | I  | V11      | System          |
| V <sub>DD</sub> CORE,<br>V <sub>DD</sub> APE, V <sub>DD</sub> IO,<br>V <sub>DD</sub> PE, V <sub>TT</sub> PE | See Table 18 for a listing of power pins.  |          |                 |
| V <sub>SS</sub>   | See Table 19 for a listing of ground pins. |          |                 |

Table 20 PES12NT3 Alphabetical Signal List (Part 3 of 3)

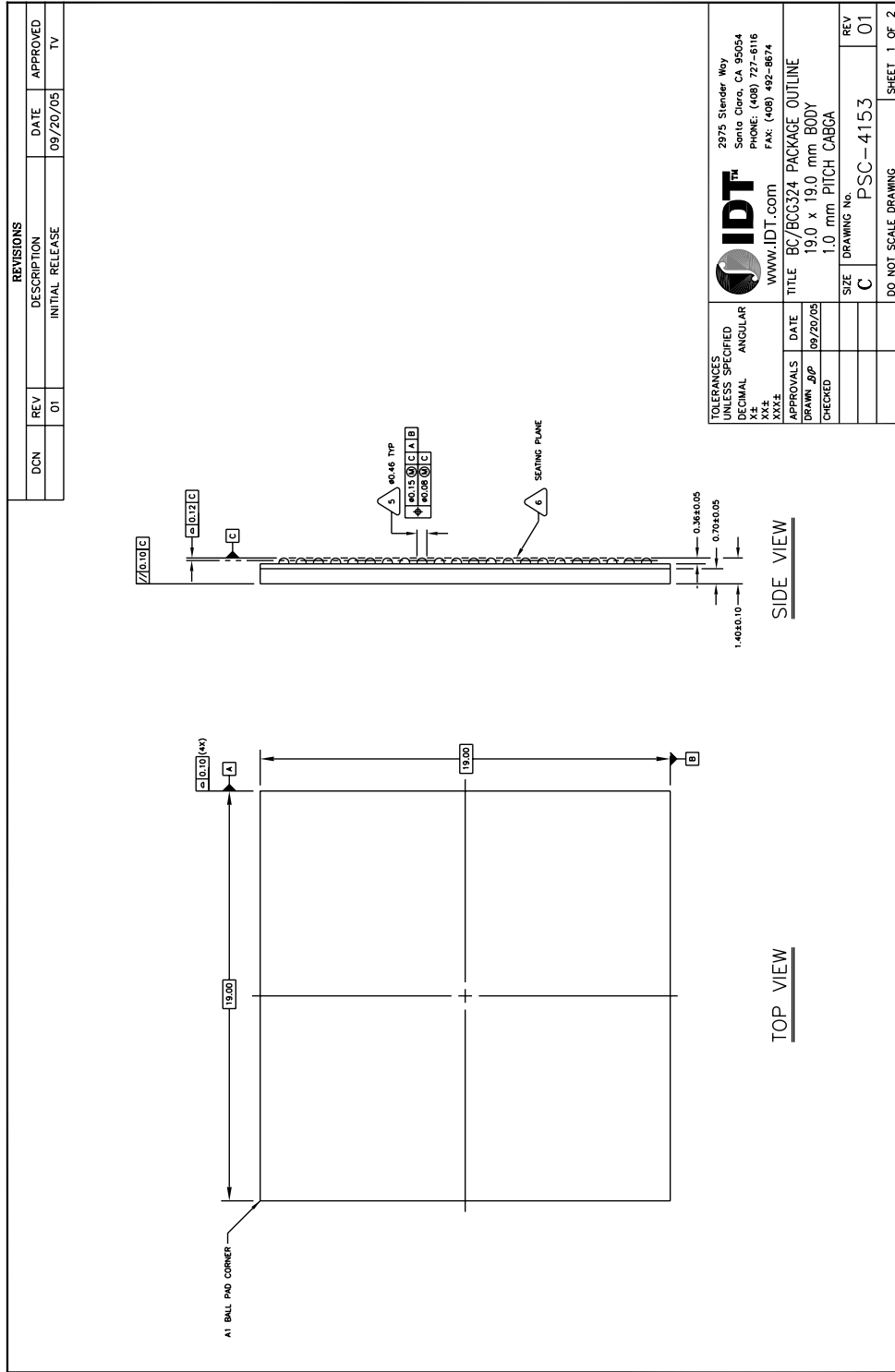


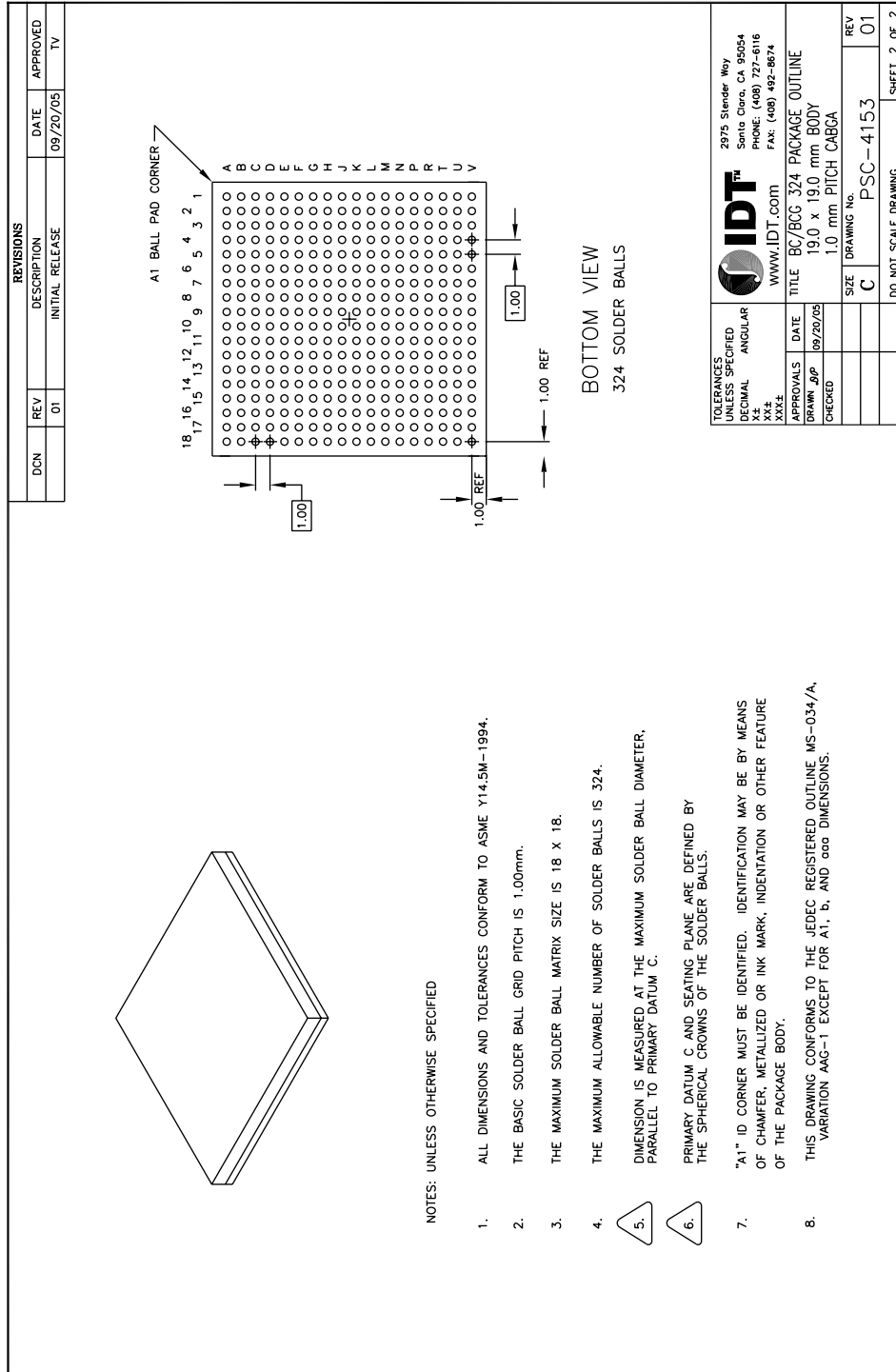
# PES12NT3 Pinout — Top View

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|
| A |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| B |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| C |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| D |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| E |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| F |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| G |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| H |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| J |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| K |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| L |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| M |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| N |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| P |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| R |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| T |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| U |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |
| V |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |

|  |                              |  |                             |  |              |  |         |
|--|------------------------------|--|-----------------------------|--|--------------|--|---------|
|  | V <sub>DD</sub> Core (Power) |  | V <sub>TT</sub> PE (Power)  |  | Vss (Ground) |  | Signals |
|  | V <sub>DD</sub> I/O (Power)  |  | V <sub>DD</sub> PE (Power)  |  |              |  |         |
|  |                              |  | V <sub>DD</sub> APE (Power) |  |              |  |         |

# PES12NT3 Package Drawing — 324-Pin BC324/BCG324





## Revision History

March 15, 2007: Initial publication of Preliminary data sheet.

April 11, 2007: In Table 2, revised description of MSMBCLK.

## Ordering Information

| Product Family | Operating Voltage | Device Family | Product Detail | Revision ID | Package | Temp Range |   |
|----------------|-------------------|---------------|----------------|-------------|---------|------------|---|
| 89             | H                 | PES           | 12NT3          | ZA          | BCG     | Blank      | Commercial Temperature (0°C to +70°C Ambient) |
|                |                   |               |                |             | BC      |            | BC324 324-ball BGA                            |
|                |                   |               |                |             | BCG     |            | BCG324 324-ball BGA, Green                    |
|                |                   |               |                |             |         |            | ZA Silicon revision                           |
|                |                   |               |                |             |         |            | 12NT3 12-lane, 3-port                         |
|                |                   |               |                |             |         |            | PES PCI Express Switch                        |
|                |                   |               |                |             |         |            | H 1.0V +/- 0.1V Core Voltage                  |
|                |                   |               |                |             |         |            | 89 Serial Switching Product                   |

**Legend**  
 A = Alpha Character  
 N = Numeric Character

### Valid Combinations

- 89HPES12NT3ZABC 324-pin BC324 package, Commercial Temperature
- 89HPES12NT3ZABCG 324-pin Green BC324 package, Commercial Temperature



**CORPORATE HEADQUARTERS**  
 6024 Silver Creek Valley Road  
 San Jose, CA 95138

**for SALES:**  
 800-345-7015 or 408-284-8200  
 fax: 408-284-2775  
[www.idt.com](http://www.idt.com)

**for Tech Support:**  
 email: [ssdhelp@idt.com](mailto:ssdhelp@idt.com)  
 phone: 408-284-8208